Diamond$_X$ HSIO

8 Lane SerDes Instrument for Testing of High-Speed Serial Interfaces

The HSIO is an 8 lane SerDes instrument that is optimized for testing clock-embedded serial interfaces commonly found in modern mobile, consumer, industrial and automotive electronics. These ports connect modems, cameras, displays, and storage to the applications processors to enable high bandwidth, low power consumption, and low EMI.

Automotive

Consumer

Flat Panel Display

IoT/IoV & Optoelectronics

Industrial & Medical

MCU

Mobility

Highlights

- Physical layer testing with built in PRBS BERT TX/RX
- BIST/DFT testing using high bandwidth drive/compare memory
- Protocol level testing using deep send and receive pattern memories

Features

- Test of high speed serial ports with data rates up to 6.4 Gpbs, such as HDMI, MIPI, JESD204, PCIexpress, SATA, EDP
- 8 differential, split I/O lanes, configured as two 4 lane ports
- Hardware clock data recovery per lane with flexible BERT sync
- Deep source and capture memory, as well as built in PRBS and 8b/10b encoding
- Per wire PMU for DC parametrics and common mode shift capability

- **SerDes**
- **8 differential TX channels**
- **8 RX Differential Channels**

- **6.4 Gb Data Rate**
- **128M TX Vector Memory Jitter Injection**
- **Eye Mask, PRBS**

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Specifications

Channels

- Channels per instrument — 8 Differential TX, 8 Differential RX

Frequency Specifications

- Time Domains per
- Instrument — 2, one time domain per 4 lanes
- UI period — 156.25 ps to 10000 ps (100 Mbps to 6.4 Gpbs)
- On-the-fly Period Change Range — 2 to 62, Even integer division of primary rate

Operating Modes

- DUT Phy Mode (PRBS, BIST) — 8 inputs and 8 outputs; up to 240K bit cell pattern depth, force and expect only
- DUT RX mode — 8 inputs; up to 128M symbols
- DUT TX mode — 8 outputs; up to 128M symbols
- DUT Duplex mode — 4 inputs and 4 outputs; up to 128M symbols, force and expect or force and capture

Pattern Specifications

- Keepalive Memory Size — 16 to 4096 UI, modulo 4 increments
- Built-In PRBS BERT — PRBS 7, 15, 23 or 31
- PRBS Seed Value — 1 to 2n+1 – 1
- History RAM — 256 symbols
- Pattern Key Match Word — 40 bits
- Sync/Training Key Word — 10 bits
- Disparity — Transmit on/off, Receive on/off
- Out of Band Signaling — On/off under pattern control

Transmitter

- Driver Min/Max Level range – DC Coupled — 0 to 1.5V
- Driver Swing range — 0.1 to 1.5V
- AC Coupled Termination Voltage Range — 0 to 3.5V
- Eye Opening at 6.4 Gbps — 60% minimum
- Programmable Pre-Emphasis Amplitude — 30 %
- Jitter Injection Range — +/-40UI

Pattern Specifications

- Clocking Mode — Embedded Clock
- Differential Input Impedance — 100 Ω
- Minimum Edge Density — 1 transition per 4096 UI
- Minimum Bit Lock Transitions — 8192 transitions
- Tracking Loop Bandwidth — 1 MHz
- Lane-Lane Deskew Range — 1000 UI
- Input Level Range — 0 to 1.5 V
- Min/Max Input Amplitude — 5 mV to 1.5 V
- AC Coupled Input Voltage Range — 0 to 3.5 V
- Vref Range — 0 to 1.5 V
- Receiver Equalization — 31 % ti 74 %
- Minimum Eye Opening Required at 6.4 Gbps — 30 %

PPMU

- Voltage Range — -1.2 V to 3.5 V
- Current Ranges — +/-8 t, +/-32 mA

All specifications are subject to change without notification and are for reference only. For detailed performance specifications, please contact Cohu.